NORTH CAROLINA AGRICULTURAL AND TECHNICAL
STATE UNIVERSITY

Department of Electrical Engineering
Greensboro, NC 27411

Technical Report

on

MATERIAL GROWTH AND CHARACTERIZATION FOR SOLID STATE DEVICES

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Submitted by:

W. J. Collis, Principal Investigator
A. Abul-Fadl
S. Iyer

MATERIAL GROWTH AND CHARACTERIZATION FOR SOLID STATE DEVICES

SUMMARY

During this report period InGaAs and InGaAsP were grown upon (100)InP by liquid phase electroepitaxy (LPEE). Results of the epitaxial growth of InGaAs on sputtered quartz masked substrates are presented. The resulting surface morphology can be related to the current density distribution near the edges of a masked pattern. The quaternary InGaAsP was grown with compositions corresponding to 1.3 μm and 1.5 μm emission wavelengths. Growth rates were found to be linearly dependent upon current density, and a strong dependence upon composition was noted. These compositions lie in the miscibility gap region of the alloy phase diagram at the 645 ^{o}C growth temperature. Growths were performed at 685 ^{o}C to avoid the miscibility gap. Epilayers were characterized by photoluminescence, X-ray diffraction, SIMS, and Hall effect measurements. Aluminum oxide was deposited upon silicon and InGaAs substrates for the characterization of this material as an insulator in a field effect transistor structures. It was determined that the results did not warrant further work with the deposition from an aluminum isopropoxide source. A metalorganic vapor phase epitaxy system installation system is nearing completion for use in hybrid III-V semiconductor epilayer growths.

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INTRODUCTION

This research report presents results of a program in semiconductor materials deposition, characterization and fabrication of electronic devices. The primary deposition process is liquid phase electroepitaxy (LPEE) of InGaAs and InGaAsP on InP substrates. (This growth process has been previously referred to as current controlled liquid phase epitaxy - CCLPE). The original proposed tasks are listed here.

TASK I:

Multilayer growths by LPEE, with an investigation of dopants and selective growth techniques. Also, hybrid multilayer growths were to be performed with a metalorganic vapor phase epitaxy system which is under development.

TASK II:

Electronic device fabrication. A MISFET device with a deposited insulator for the gate was to be fabricated, if a feasible deposition process could be developed.

TASK III:

Fabrication for a p-i-n photodiode for sensor applications. This structure would utilize a selective mesa growth and a diffused junction.

These goals have been modified throughout the contract period to reflect changes in process techniques, funding and personnel expertise. In the next section, the various technical results will be presented. Appendix A contains abstracts of five theses completed by M.S.E.E students during this reporting period.

TECHNICAL DISCUSSION

In this section the various results of the research activities during this reporting period are presented.

A. Selective Area Growth of InGaAs

The growth of InGaAs in localized regions of an InP substrate was investigated as a means of creating device mesa structures or isolated dopant regions. Growth or etchback can be achieved by reversing the current direction. Thus, trenches can be formed in the substrate surface and then refilled with another lattice-matched semiconductor compound or alloy. The masking material must be able to withstand the growth temperature cycling and be a suitable, non-contaminating electrical insulator. Ion beam sputtered quartz (SiO_2) has been used for the mask in this work.

Selective growth of InGaAs islands on SiO_2-masked Fe-doped (100) InP substrates was performed by liquid phase electroepitaxy. The growth of the layer was done at a constant furnace temperature of 640°C by passing a direct electric current from the substrate to the melt. The current density used was 1 to 5 A/cm^2 for a period of 15 minutes. The isolated InP regions were of various sizes (80 x 100μm to 3000 x 3000μm), and different geometries (narrow and wide strips, square, circular). A uniform growth with excellent surface morphology (no terraces or voids or defects) was obtained on strips as wide as 200μm and on circles with diameters less than 500μm. Figure 1 is photomicrograph of two narrow strips 150 x 3000μm each. The figure clearly shows a terrace-free surface with no voids or defects or other features. Figure 2 is a photomicrograph of a cleaved section of one of the strips shown in Fig. 1. The figure shows the uniformity of the layer. The shape of the growth layer that protruded from the substrate coincided with the mask pattern and the sides of the layer are perpendicular to the <111> directions (about 54.8° angle with the (100) substrate).

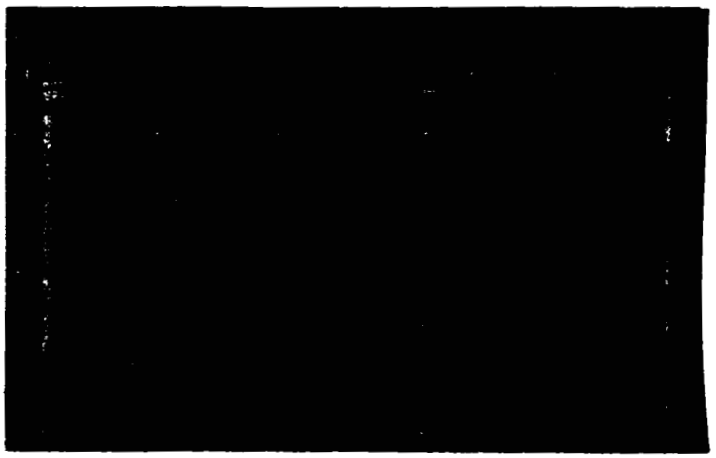

Figure 1. Surface morphology of InGaAs epilayer grown on a narrow strip geometry at 640 ^{o}C and 1 A/cm^{2} for 15 minutes.

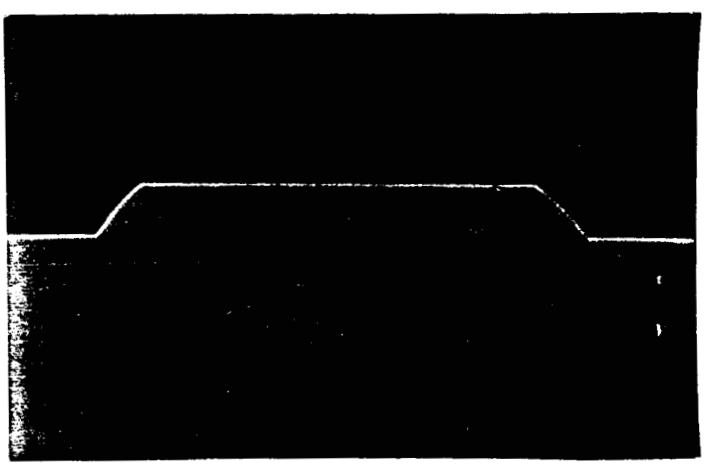

Figure 2. Cleaved section of the narrow strip shown in Fig. 1. The layer is about 17 μm thick and 150 μm wide.

For islands with wider geometry, the growth was uniform up to 100-200μm from the periphery with excellent surface morphology. However, the central region was slightly thinner and the surface morphology was of inferior quality. Figure 3 is a photomicrograph of a wide strip (780x 2000μm).

The uniformity of the growth is attributed to the uniformity of the electric field along the substrate melt interface (S-M). A mathematical model of the substrate, back-contact melt, growth melt, and SiO_2-mask, shown in Fig. 4, is used to investigate the uniformity of the electric field along the S-M interface. Numerical solution of the field equation for different geometries is done by the finite element method. The computer simulation results of the model for narrow and wide geometry as well as other experimental results are presented in Appendix B ("Selective Electroepitaxial Growth of $In_{0.53}Ga_{0.47}As$ on (100) - Fe:InP"). This paper will be presented during the 1987 SOUTHEASTCON in Tampa, Florida, April 5-8, 1987.

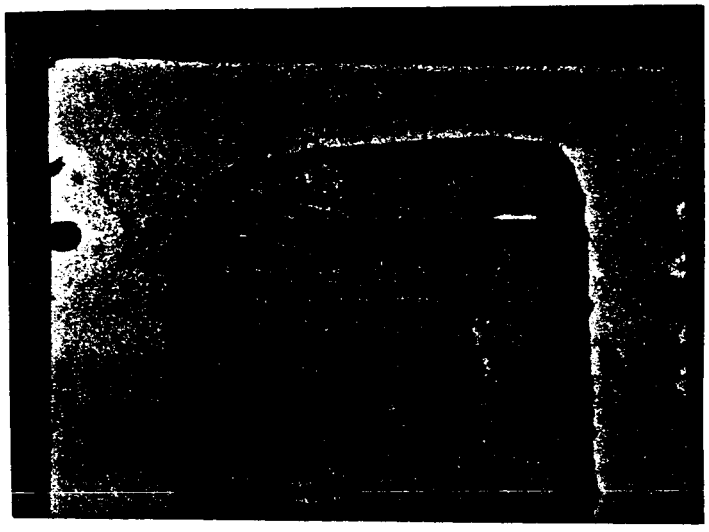

Figure 3. Surface morphology of InGaAs epilayer grown on a wide strip geometry at 640 ^{o}C and 1 A/cm^{2} for 15 minutes.

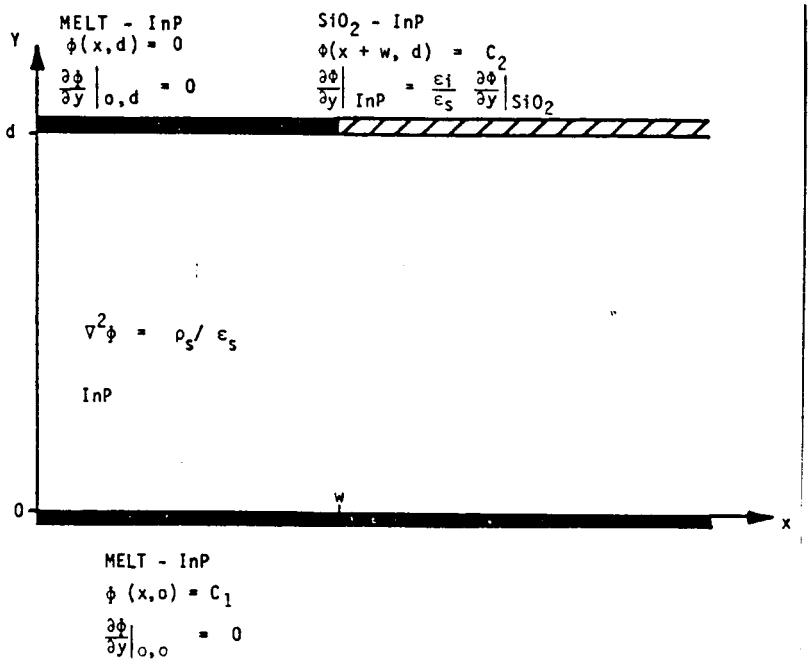

Figure 4. Schematic cross-section of the substrate, growth melt and back contact melt model used to analyze selective epitaxy.

B. Growth and Characterization of InGaAsP

$In_{1-x}Ga_xAs_yP_{1-y}$ quaternary alloys with compositions corresponding to 1.31μm and 1.52μm have been studied in detail[14]. These alloys have applications in devices for optical fiber communications since the fibers exhibit desirable transmission and dispersion properties in these wavelength regions.

The epitaxial InGaAsP layers were grown lattice matched to (100) InP substrates using the LPEE technique at 645°C. The melt composition calculations were based upon information for the InGaAsP system by Hsieh [1]. Two solidus compositions were grown: $In_{.60}Ga_{.40}As_{.85}P_{.15}$ ($In_{.60}$, $\lambda = 1.52\mu m$) and $In_{.73}Ga_{.27}As_{.60}P_{.40}$ ($In_{.73}$, $\lambda = 1.31\mu m$). Growths were performed at a constant furnace temperature of 647°C with a direct current density of 3 to 15 amp/cm^2.

The variation of growth rate as a function of current density and composition was studied. In general, the growth rate of the epilayer was found to be linearly dependent on current density for both compositions. However, for $In_{.73}$ the growth rate was found to be non-linear at low current densities. The growth rate was found to be a function of the composition of the quaternary layers. The growth rate of the $In_{.60}$ layers was almost six times larger than that of the $In_{.73}$ layers. Furthermore, layers thicker than 3μm could not be grown. The low growth rate of these materials could be attributed to the fact that these compositions lie in the miscibility gap region. The growth velocity behavior with alloy composition is shown in Fig. 5. Literature data for step and equilibrium cooling growth of the quaternary are also indicated in this figure.

The lattice mismatch between the epilayer and the substrate was determined by the single crystal X-ray diffraction technique. For the $In_{.73}$ layers a good match with $\Delta a/a = 0.04\%$ was obtained, whereas for the $In_{.60}$ samples an

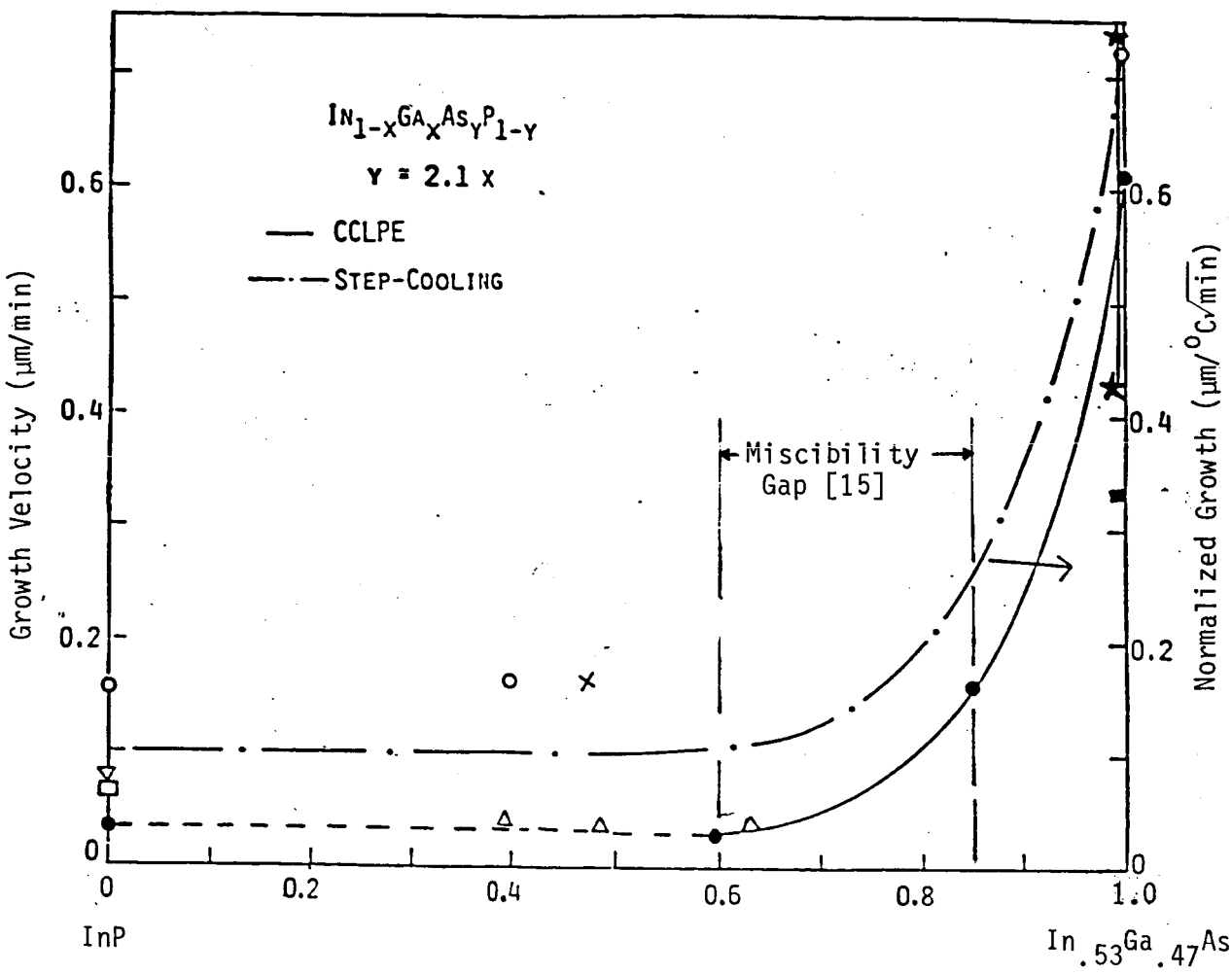

Figure 5. Normalized growth rate vs. alloy composition. Growth velocities from literature data are also shown.

Step-cooling: o Cook, et al. [2], x Kunishige, et al. [3], Δ Feng, et al. [4], □ Ishibashi, et al. [5], ▽ Hsieh, et al. [1].

Equilibrium cooling: * Amano, et al. [6], ■ Pearsall, et al. [7]

LPEE: ● This work.

increase in lattice mismatch with consecutive growth runs from the same melt was observed. Room temperature photoluminescence measurements were also performed. The $In_{.60}$ samples exhibited a systematic shift in peak wavelength for consecutive growths from 1.56μm to 1.49μm. However, the $In_{.73}$ layers only shifted in wavelength from 1.33μm to 1.31μm for consecutive growths.

Electrical characterization was done by performing Hall measurements at room temperature. The Hall mobilities for the unintentionally doped quaternary layers were in the range of 3900 to 5680 $cm^2/V\text{-}sec$. The carrier concentration was typically in the low $10^{17}cm^{-3}$ range.

In order to avoid the miscibility gap in the phase diagram, growths of the 1.3μm alloy were performed at 685°C. Various melt baking sequences were tried in order to reduce the residual carrier concentration. A low concentration of $2 \times 10^{16}cm^{-3}$ was achieved but not consistently. The graphite boat components were sent to Poco Graphite for high temperature purification. A water vapor monitor was used on the reaction tube exhaust connection to optimize the post-loading purge cycle and the melt baking time. Care was also taken to minimize the exposure of the graphite to the atmosphere during the loading sequence, thus reducing the adsorption of water vapor.

The epilayers were grown at a temperature of 685°C for periods ranging from 30 to 90 minutes, with thicknesses in the range of 1.5 to 18μm. The growth rate of the epilayers was found to be linearly dependent on the current density, which ranged from 6.5 to 12.0 $amps/cm^2$. The surface morphology, in general, exhibited a fine terracing which is characteristic of LPEE grown layers. Photoluminescence measurements performed on these samples indicated no significant shift in the peak wavelength (<150 Å) for the layers grown in consecutive runs using the same melt. This suggests a homogeneous composition of the epilayer. Single crystal X-ray diffraction measurements indicated narrow diffraction peaks consistent with a uniform composition through the

epilayer thickness, with a lattice mismatch of less than 0.03%. However, the samples grown from melts with extensive baking for purification or excess InAs resulted in positive lattice mismatches of 0.3%. These latter results are in agreement with photoluminescence measurements in which a large growth-to-growth shift in the peak wavelength toward longer wavelength has been observed.

Chemical etching of the samples, using the A-B and H-etch solutions [8], helped to reveal defects which appeared as etch pits and dislocation lines on the epilayer surface donot appear to originate in the substrate material, thus indicating that they are formed as a result of the lattice mismatch between the substrate and the epilayer.

Secondary ion mass spectroscopy (SIMS) measurements indicated a uniform composition of the lattice matched epilayers within the experimental error of ±10%. These measurements were performed at North Carolina State University. However, no quantitative conclusion about the composition of the epilayers could be drawn since, depending on the ion source used, the ion yields of either In and Ga, or As and P varied over a wide range on the same sample.

Hall measurements using the van der Pauw technique were performed to obtain electrical characterization of the samples. High purity quaternary layers with carrier concentrations 9×10^{15} cm^{-3} and Hall mobilities of $4{,}400 cm^2/V\text{-sec}$ at room temperature have been obtained. Epilayers are presently being doped with Mn, resulting in p-type material with carrier concentrations $2 \times 10^{17} cm^{-3}$.

C. Deposition of Aluminum Oxide for Insulator Applications

This task objective was directed toward developing a suitable insulator deposition process for fabricating MISFET (insulated gate FET) structures on epitaxial InGaAs. The III-V compound semiconductors have generally exhibited poor interface characteristics with respect to the typical choices of

deposited insulators; e.g., SiO_2 and Si_3N_4. Aluminum oxide was chosen because a chemical vapor deposition process utilizing aluminum isopropoxide as the source was easily implemented. This type of deposited film may be useful also as a masking layer in a processing sequence.

Typical deposition conditions were: argon carrier and purge gas, about 2 liters/min total flow in a 50 mm diameter quartz tube, 325-375°C susceptor temperature, source bubbler at 125°C. Both cold wall (with the susceptor heated with an external tungsten lamp) and hot wall furnace systems were tried. The latter resulted in a much heavier deposit upon the reaction tube surface. This appeared to contaminate the sample surface with dust particles.

Deposition of $A\ell_2O_3$ was performed on Si and InGaAs substrates, the former being chosen for economy. The quality of the insulator interface with the semiconductor was inferred from the capacitance-voltage (C-V) data obtained at 1MHz. Somewhat classical C-V data were obtained for the Si substrates, with an apparent flatband voltage which was quite small (on the order of a few volts) considering the lack of special precautions to avoid sodium ion contamination. A feature of all of the C-V data to some extent was a hysteresis in the anticipated depletion regime of the C-V characteristics. Typically this hysteresis exhibited a clockwise sense for low rates of change of the gate bias. When the magnitude of the gate bias slope exceeded approximately 100mV/sec, the hysteresis loop would collapse, then expand in the counter-clockwise sense as the rate of change was increased. This hysteresis effect can be related to the difficulties observed by others in attempting to use this deposited alumina as the gate insulator in MISFETs [9,10]. In those cases the drain current was observed to decay after the application of a gate bias to turn the device on. This drifting effect was effectively eliminated by performing an <u>in situ</u> native oxide etching operation using a high

concentration of HCℓ vapor before beginning the $Aℓ_2O_3$ deposition from the aluminum isopropoxide source [11]. A system was assembled to thermally decompose $MoCℓ_5$ in hydrogen at 900°C to serve as a source of HCℓ. While there was evidence of HCℓ generation with this system, it was not easily controlled in operation. Thus, the attempt to use chemically generated HCℓ was abandoned. The use of anhydrous HCℓ in a carrier gas was not feasible during this research effort because of the lack of a suitable exhausted enclosure for the deposition apparatus.

The behavior of a MIS capacitor fabricated on n-type Si is illustrated by the C-V data shown in Fig. 6. The initial hysteresis loop width (A) is about 7.5 volts wide. After annealing this sample in nitrogen at 350°C for one hour the loop width (B) had decreased to about 3.2 volts. These curves were recorded at a bias sweep rate of 450 mV/sec and a frequency of 1MHz.

Aluminum oxide layers were also deposited on epitaxial layers of InGaAs on InP. The Aℓ-$Aℓ_2O_3$ - pInGaAs MIS capacitor C-V data are shown in Fig. 7 (4.5 V/sec, 1 MHz). The p-type InGaAs had a hole concentration of about $2 \times 10^{17} cm^{-3}$. There is still a hysteresis effect and the capacitance change is much smaller than in the Si case because of the higher carrier concentration in the InGaAs.

The cause of the hysteresis effects is apparently an interface state condition between the deposited oxide and the semiconductor surface. This is a function of the type of semiconductor, of course and the condition of its surface at the time of the insulator deposition. In the case of InP, surface decomposition can occur even though the deposition temperature for the aluminum isopropoxide process is in the 300-400°C range. In the current work there appeared to be a great variability in the deposition rate and the quality of the oxides from one deposition run to the next. This may be the

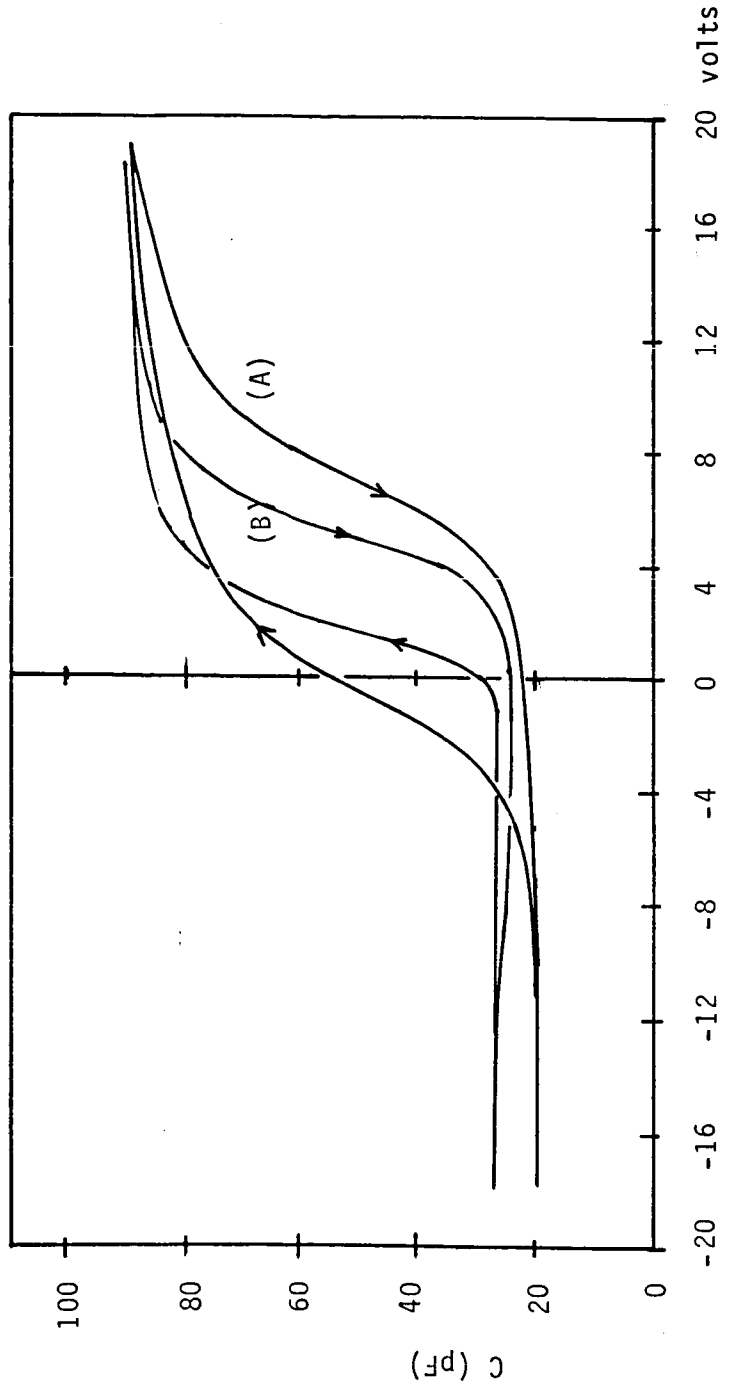

Figure 6. C-V characteristics of an Al-Al_2O_3-nSi capacitor measured at 1 MHz. Bias sweep rate is 0.45 V/s. Curve A is as-formed device. Curve B is after annealing in nitrogen for 1 hour at 350 ^{o}C.

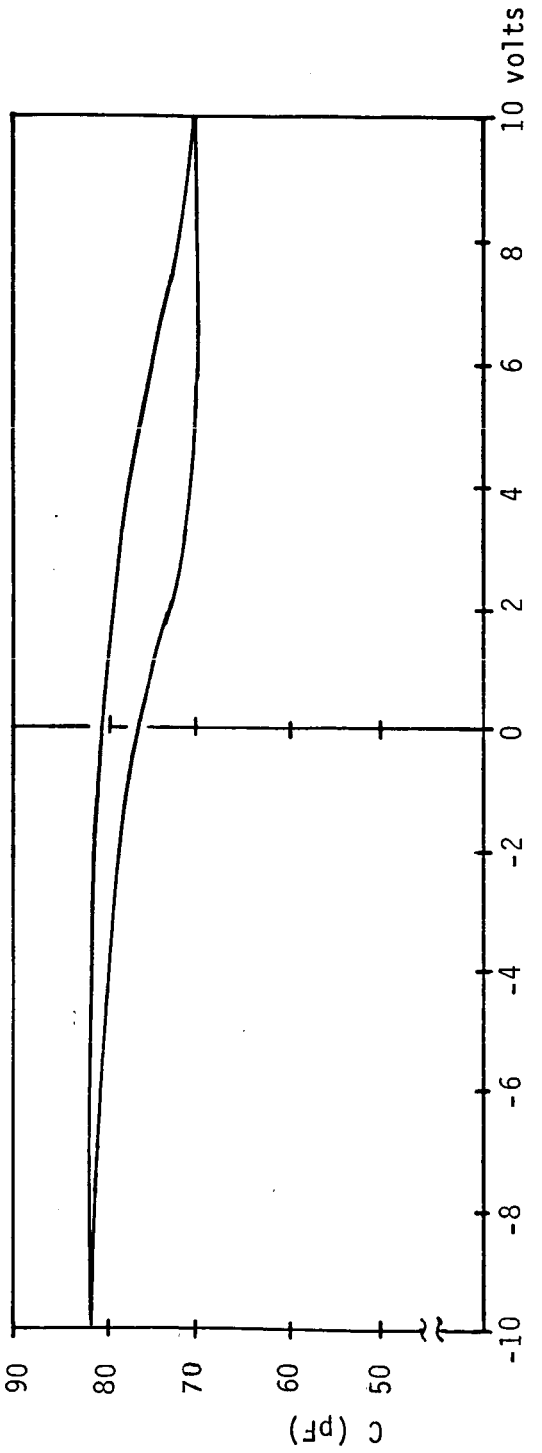

Figure 7. C-V characteristics of an Al-Al_2O_3-pInGaAs capacitor measured at 1 MHz. Bias sweep rate is 4.5 V/s.

result of variation in the concentration of the reactant vapor in the carrier gas entering the susceptor region. An excessive amount of vapor may not completely decompose at the substrate surface. The etching behavior of the oxide layers varied greatly, also, Some layers appeared to dissolve very quickly in buffered hydrofluoric acid, while other samples would require an hour in 48% HF to remove all of the deposited layer. There were isolated islands which dissolved very slowly. Figure 8 is a scanning electron microscope photomicrograph of a layer of deposited $A\ell_2O_3$ partially etched for 3 minutes in buffered hydrofluoric acid. A masked, unetched region of the oxide layer is visible at the right edge of the figure. The faceted appearance suggests that the material has deposited in the form of micro-crystallites. The variation of etching with distance from the edge of the thick wax mask is an unexpected result.

The use of $A\ell_2O_3$ pyrolytically deposited from aluminum isopropoxide as a gate insulator in a MISFET device is no longer considered as a viable process in this Laboratory. The process may be useful in various processing steps requiring a mask or insulating layer. A more controlled process with the added capability of semiconductor surface modification is required for the satisfactory fabrication of III-V MISFET structures. Various plasma enchanced, or remote plasma systems appear to yield the most promising results. Aluminum oxide has also been deposited by the oxidation of trimethyalumium (TMA1) [11,12]. Since we are currently developing a metalorganic vapor phase epitaxy system, it may be convenient to implement such an oxide deposition system.

The success of an insulated gate device depends on a great extent upon the quality of the interface between the insulator and the semiconductor. This quality is affected by many chemical and physical factors which are related to the materials selected and the fabrication process. In the case

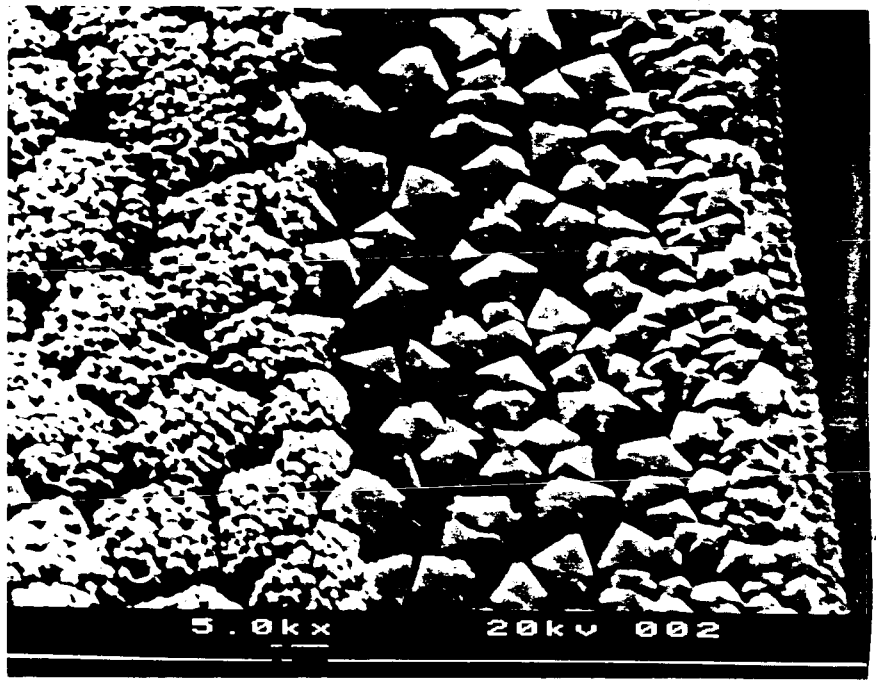

Figure 8. Deposited layer of Al_2O_3 on Si partially etched by buffered HF for 3 min. The longer marker is 1 μm.

of the III-V semiconducting compounds or alloys, the insulator growth or deposition temperature must be low enough to prevent thermal decomposition of the semiconductor surface. The nature of this surface is critical during the initial stages of deposition. Loss of the Group V constituent results in a metal-rich interface region. Native oxides present or formed during the deposition of the insulator generally result in an unstable device behavior, with the instability resulting from the time response of interface trapping states. Native oxides of the III-V semiconductors also tend to decompose at moderate processing temperatures, again leaving Group III or Group V-rich interfacial layers. A good review of semiconductor interfaces is presented by Wilmsen [13].

D. Metalorganic Vapor Phase Epitaxy System

This research in optoelectronic device materials was to be complemented by hybrid growths in conjunction with a metalorganic vapor phase epitaxy (MOVPE) system which is being developed in our Laboratory. This is a vertical, atmospheric pressure system with two Group III alkyl control channels and a Group V hydride channel. The system installation has required considerable time-consuming laboratory/building modifications. Funds from this research grant have been used to provide exhaust systems for the MOVPE reactor and chemical fume hood. It is now at the stage of completing the control and safety interlock/alarm system. The intention is to employ LPEE and MOVPE as complementary growth techniques to achieve high purity by LPEE and particular sequences, such as InP on InGaAs, by MOVPE. (The latter ternary growth is not possible with LPEE because of the dissolution of the ternary layer.) Since the system is not currently configured to accommodate phosphine injection, this application will have to await further system development funding.

E. Future Plans

During the remaining grant period efforts will continue in the materials growth and characterization areas. The masked LPEE growth of the ternary InGaAs on InP will continue with a study also of the process of etching achieved by reversing the current direction. P-n junctions formed in these masked regions will be characterized electrically.

The quaternary InGaAsP material is being doped with manganese. Low temperature Hall effect and photoluminescence measurements are being performed to determine the prevalent scattering mechanisms in these films.

The MOVPE system will soon be ready for operation. The first growths will be GaAs in order to establish the systems operating characteristics and the purity capability. Proposals are being prepared to modify the MOVPE system with the addition of indium and phosphine source channels, and a new injection port to make abrupt multilayer structures possible.

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APPENDIX A

THESES ABSTRACTS

GROWTH AND CHARACTERIZATION OF Mn-DOPED AND UNDOPED InGaAs/InP USING CURRENT CONTROLLED LIQUID PHASE EPITAXY

by Sami M. Kadamani

(Dr. A. Abul-Fadl, Advisor)

In this study, the results of growth and characterization of undoped(n-type) and Mn-doped(p-type) $In_{0.53}Ga_{0.47}As$ layers on Fe-doped(semi-insulated) and Sn-doped(n-type) (100)InP, using current controlled liquid phase epitaxy (CCLPE), were presented. Growth was performed at a constant furnace temperature of 640 ^{o}C by passing direct electric current of 2.5 to 10 A/cm^{2} across the substrate-melt (S-M) interface, for periods ranging from 15 to 60 minutes. The average growth velocity showed a linear dependence on the current density.

Mn-diffusion occurred during growth of the epitaxial layer on Fe-doped InP. However, when Mn-doped layers were grown on Sn-doped InP, no diffused layers were observed.

Electrical characterization of the grown and diffused layer was done using Hall measurements at room temperature. The undoped InGaAs layers exhibited carrier concentrations in the range of

0.87×10^{16} /cm^3 to 6.42×10^{16} /cm^3. While those of the Mn-doped layers were higher, in the range of 1.75×10^{17} /cm^3 to 6.04×10^{17} /cm^3. Hall measurements also showed that the average carrier concentration of the diffused layer was about two orders of magnitude below that of the epilayer.

SIMS analysis was performed for further characterization of the Mn-diffusion into semi-insulating Fe-doped InP.

SELECTIVE ELECTROEPITAXIAL GROWTH OF $In_{0.53}Ga_{0.47}As$ ON (100) Fe-doped Inp

by Samir M. Maanaki

(Dr. Ali Abul-fadl, Advisor)

Electroepitaxy has been used to grow InGaAs on selected (100) InP islands using a sputtered SiO_2 layer as the substrate mask. The growth was performed by passing low direct electric current of 1A for 15 minutes across the substrate-melt interface with a constant furnace temperature of 640 °C. The epitaxial layers were characterized with respect to their surface morphology and thickness uniformity. It was found from the experimental results that a uniform layer with excellent surface morphology can be achieved on small regions as wide as 200μm and on circles with diameter of less than 500μm. Also it was found that the electric field intensity along the substrate-melt interface of the islands is dependent upon the geometry of the growth regions. Poisson's equation was solved by the finite element method to show the relation between the intensity of the field and the uniformity of growth in various regions.

PREPARATION AND PROPERTIES OF CVD ALUMINUM OXIDE FILMS ON III-V SEMICONDUCTORS FOR MISFET APPLICATIONS

By Zongyi Cheng

(Dr. W. J. Collis, Advisor)

This research has been concerned with the development of improved fabrication and measurement techniques for a metal-insulator-semiconductor field effect transistor(MISFET). Specifically, aluminum oxide films were chosen for this investigation because high quality films of Al_2O_3 have been shown to have a high resistivity and breakdown field. Aluminum oxide films were deposited on substrates for this study by chemical vapor deposition(CVD). Recently in our work, the construction of a hot wall CVD system was completed and aluminum oxide films were deposited by chemical vapor deposition at 320°C. The aluminum oxide films were initially deposited on silicon and later on InP and InGaAs. The temperature and flow rate were strictly controlled during CVD process. Film defects were reduced by filtering the reactant gases.

The capacitance-voltage(CV) measurements were made on the metal-insulator-semiconductor(MIS) structures to determine the electrical characteristics. The following data are experimental results:

a) Hysteresis is present in all of the C-V curves as the gate voltage is cyclically changed from positive to negative.

b) The width of the hysteresis loop observed in the C-V curves was found to be dependent upon the bias sweep rate.

c) As the bias voltage sweep rate was increased, the width of hysteresis would first decrease to zero and then increase.

d) The gate bias was swept at a rate of 4.5 to 0.04 v/sec (dv/dt) for a maximum voltage excursion of ±20V.

e) After an annealing process, the width of hysteresis become smaller, the higher the annealing temperature, the smaller the hysteresis width.

Further improvements in MIS capacitor performance will depend upon the quality of the deposited films and the reduction of interface states.

CURRENT CONTROLLED LIQUID PHASE EPITAXIAL (CCLPE) GROWTH AND CHARACTERIZATION OF InGaAsP (λ = 1.3 μm) on (100) InP

Lynora Camille Jones

(Dr. Shanthi Iyer, Advisor)

In this thesis research, InGaAsP grown on InP substrates at an energy gap corresponding to a peak wavelength of 1.3 μm has been reported using the current controlled liquid phase epitaxy technique. The layers were grown at a constant furnace temperature of 685°C by passing an electric current from the substrate to the melt for periods ranging from 30 to 90 minutes. The growth results showed a linear relationship between the growth rate of the quaternary epilayer and current density (6.5 to 12 A/cm^2). The thicknesses of the epilayers measured were in the range of 1.5 to 18 μm.

The above technique produced high purity layers of good quality and fine terraced surface morphology. Chemical etching of the samples, using the A-B and H-etch solutions, helped to reveal defects which after etching, appeared as etch pits and dislocation lines on the epilayer. X-ray diffraction measurement showed good lattice match between the epilayer and substrate. A lattice mismatch as small as 0.00027 was obtained. Photoluminescence measurements performed on the samples showed a peak wavelength which varied from 1.2 to 1.3 μm

depending on the history of the baking cycle. These measurements indicated no signficant shift (<150 Å) for the layers grown from consecutive runs of the same melt indicating a uniform composition of the layer. Although SIMS analysis measurements indicated uniform composition of the layer, no definite quantitative conclusion on the composition could be drawn. Room temperature Hall measurements resulted in a Hall mobility and carrier concentration in the range of 1040 to 4280 $cm^2/V\text{-}sec$ and 1 x 10^{17} to 2 x $10^{16}/cm^2$, respectively.

GROWTH AND CHARACTERIZATION OF InGaAsP ON (100)InP SUBSTRATES BY CURRENT CONTROLLED LIQUID PHASE EPITAXY

by Sai S. Vallabha

(Dr. Elias K. Stefanakos, Adviser)

In this investigation, the growth of InGaAsP layers lattice matched to (100)InP substrates is reported for the first time using the current controlled liquid phase epitaxy technique. The layers were grown at a constant furnace temperature of 647 °C for periods ranging from 15 minutes to 2 hours, with a direct current of 3A/cm^2 to 15A/cm^2. The layers grown corresponded to the two solidus compositions, $In_{0.60}Ga_{0.40}As_{0.85}P_{0.15}$ (λ =1.52μm) and $In_{0.73}Ga_{0.27}As_{0.60}P_{0.40}$ (λ =1.31μm). The growth rate of the epilayer was found to be linearly dependent on current density for both of these compositions. Further, the growth rate was found to be a function of the composition of the quaternary layers. It was observed that the growth rate of $In_{0.60}Ga_{0.40}As_{0.85}P_{0.15}$ layers was almost six times larger than that of $In_{0.73}Ga_{0.27}As_{0.60}P_{0.40}$ layers. The thickness of the epilayers characterized were in the range of 1.4-5.0μm and 1.4-3.0μm respectively.

Lattice mismatch between the epilayer and the substrate was determined by the X-ray diffraction technique. For $In_{0.73}Ga_{0.27}As_{0.60}P_{0.40}$ layers a good lattice match with $\Delta a/a=0.04\%$ was obtained, whereas for $In_{0.60}Ga_{0.40}As_{0.85}P_{0.15}$ samples an increase in lattice mismatch with the growth run was observed.

Photoluminescence measurements were performed to determine the energy gap and composition of the epilayers. For $In_{0.60}Ga_{0.40}As_{0.85}P_{0.15}$, a systematic shift in wavelength was observed indicating a change in the composition of the quaternary layer. The photoluminescence peak shifted from 1.56μm to 1.49μm using the same melt indicating a maximum shift of 700Å. However, for $In_{0.73}Ga_{0.27}As_{0.60}P_{0.40}$ layers using the same melt, the maximum wavelength shift was only 200Å from 1.33μm to 1.31μm.

The surface morphology was examined using a Zeiss optical microscope. The surface morphology for $In_{0.60}Ga_{0.40}As_{0.85}P_{0.15}$ samples exhibited fine terracing(λ=1.56μm). As the same growth melt was used for consecutive runs a cross-hatched pattern due to generation of misfit dislocations was observed(λ=1.49μm). The $In_{0.73}Ga_{0.27}As_{0.60}P_{0.40}$ samples also exhibited fine terracing, but as the same melt was used for consecutive runs, a rough surface was obtained due to inhibition of growth as a result of increased lattice mismatch and also due to depletion of the solute at the interface. Thus, surface morphology was found to be sensitive to lattice mismatch. These results were also found consistent with X-ray results. The electrical characterization was done by performing Hall measurements at room temperature. The resistivity and mobility of the quaternary layers were in the range of 9.22×10^{-3} to 11.10×10^{-3} ohm-cm. and 3907 to 5689 $cm^2/V\text{-}sec$, respectively. The carrier concentration was found to be typically, 10^{17} $/cm^3$.

APPENDIX B

PRESENTATION

SELECTIVE ELECTROEPITAXIAL GROWTH OF $In_{0.53}Ga_{0.47}As$ ON (100) - Fe:InP

ALI ABUL-FADL, SAMIR MAANAKI, WARD COLLIS and SHANTHI IYER

North Carolina A&T State University
Department of Electrical Engineering
Greensboro, North Carolina 27411

Abstract

Electroepitaxy has been used to grow InGaAs on selected (100) InP islands using a sputtered SiO_2 layer as the substrate mask. The epitaxial layers were characterized with respect to their surface morphology and thickness uniformity. The electric field intensity along the substrate melt (S-M) interface of the islands is found by solving the field equation by the finite element method. Experimental results show that the uniformity of the grown islands can be directly related to the uniformity of the electric field along the S-M interface.

Introduction

Studies on selective epitaxial growth within windows and on etched substrates have been reported by several investigators [1-10]. The interest in the selective epitaxial growth into the window opening of a mask lies with the inherent capability of establishing isolated areas of epitaxial regions. These regions have the potential to realize two- and three-dimensional devices for the fabrication of optoelectronic integrated circuits. Several growth techniques have been used to grow selectively on InP [1-5] and GaAs [6-10] substrates, since these materials are the basis for many semiconductor devices employed in glass-fiber communication systems for the wave length ranges from 1.2 to 1.6μm and 0.85 to 1.1μm. The growth techniques include liquid phase epitaxy (LPE) [1-4], LPE electroepitaxy (LPEE) [5], organometalic chemical vapor deposition (OMCVD) [7], vapor phase epitaxy (VPE) [8] and molecular beam epitaxy (MBE) [9,10].

This study was undertaken to investigate the growth morphology of layers of InGaAs grown selectively on SiO_2-masked Fe-doped InP substrates. The growth was performed by electroepitaxy (LPEE) at a constant furnace temperature by passing a direct electric current from the substrate to the melt.

A mathematical model of electroepitaxy was also developed and a solution for Poisson's equation in the substrate and along the substrate-melt interface was obtained using the finite element method.

Experimental Procedure

The selective growth of InGaAs was carried out in a modified LPE apparatus with a sliding graphite boat, described elsewhere [11]. The samples used in this study were (100) semi-insulating (iron-doped) InP substrates (12 x 12mm and about 400μm thick). They were cleaned with organic solvents using warm trichloroethylene (TCE), acetone and methanol. The masking pattern was first formed in a photoresist layer. A sputter deposited SiO_2 layer (1000 - 2800 Å) was then applied to the exposed areas and finally the photoresist was removed by acetone, leaving behind the SiO_2 mask. The InP islands defined by the SiO_2 mask were of various sizes (80 x 1000μm to 3000 x 3000μm) and different geometries (narrow and wide strips, square, circular) The patterned substrate was then cleaned with organic solvents and stir etched with a 1% Br-methanol before it was loaded into the growth boat.

The growth was performed at a constant furnace temperature of 640°C by passing a direct electric current of $1\ A/cm^2$ for a period of 15 minutes. Although the semi-insulating substrates have a room temperature resistivity exceeding $10^7\Omega$-cm, at the growth temperature (640°C) the conductivity is adequate for LPEE to be performed. At this temperature, the intrinsic carrier concentration is about $5 \times 10^{16}/cm^3$. In addition, it is also possible that deep impurity levels in the semi-insulating substrate are ionized, tending to increase the conductivity further. Experimental measurements of the substrate resistance at the growth temperature resulted in about 60 mΩ.

After growth the substrate was removed from the growth apparatus and the layer was examined by interference contrast microscopy. The morphology and uniformity of the layers were studied by cleaving and etching several samples with $K_3Fe(CN)_6$:KOH:H_2O solution to delineate the growth layer from the substrate.

Experimental Results

Typical surface morphology of the selectively grown layers are shown in figures 1, 2, and 3. Figures 1 and 2 are photomicrographs of a narrow strip (150 x 1000μm) and a circular area with a radius of 250μm respectively. Figure 3 is a photomicrograph of a wide strip (780 x 2000μm). Figures 1 and 2 clearly show terrace-free surfaces with no voids or defects or other features. In figure 3 the surface morphology is similar to those in figures 1 and 2

except for the central region where the layer is about 3.7μm thinner and of inferior quality. The abnormal growth in the central region of the wide strip geometries is attributed to non-uniformity of the electric field.

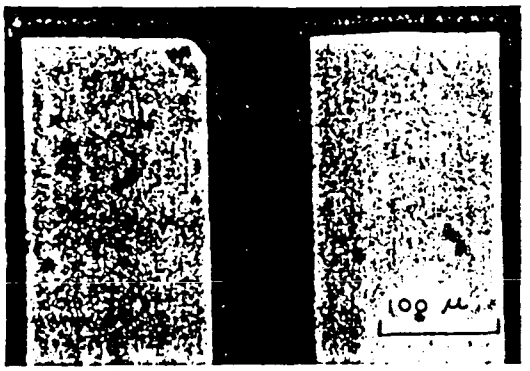

Figure 1. Surface morphology of InGaAs epilayer grown on a narrow strip geometry at 640°C and 1A/cm^2-15 minutes.

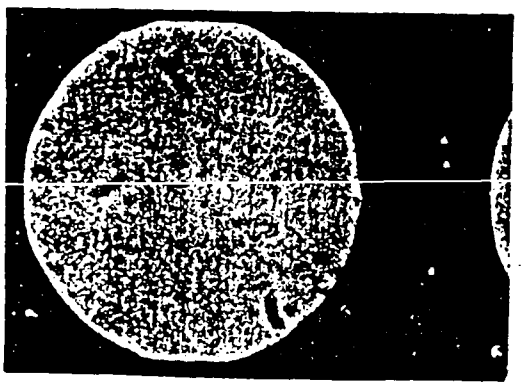

Figure 2. Surface morphology of InGaAs epilayer grown on a circular geometry at 640°C and 1A for 15 minutes.

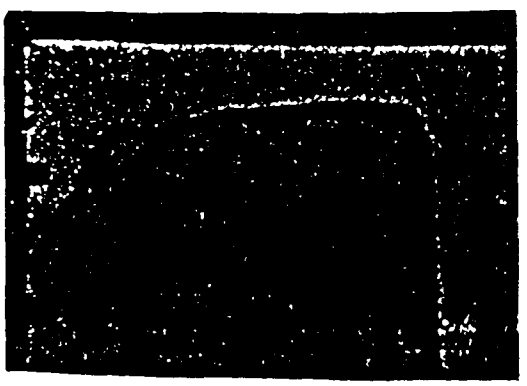

Figure 3. Surface morphology of InGaAs epilayer grown on a wide strip geometry at 640°C and 1A for 15 minutes.

Figure 4 is a photomicrograph of a cleaved section of the layer shown in figure 1. The figure shows a 1.2μm etched layer from the substrate and the grown layer. The shape of the growth layer that protruded from the substrate coincided with the mask pattern and the sides of the layer are perpendicular to the <111> directions (about 54.8° angle with the (100) surface).

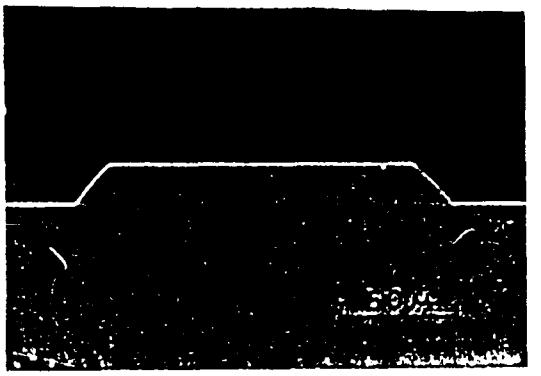

Figure 4. Cleaved section of the narrow strip shown in Fig. 1. The layer is about 17μm thick and 150μm wide.

Figure 5 shown two narrow strips, side-by-side. The strips are about 80μm wide and about twice as thick as the layer shown in figure 4. The shape of the cross-section is trapezoidal and the side walls are determined to be (111) planes. The photographs also show that the layer-substrate interface is smooth in all cleaved sections and all undercutting by the chemical etching of the substrate is completely filled with the growth layer.

Figure 5. Cleaved section of two narrow strips side-by-side. The one strip is about 80μm wide and 45μm thick and the other strip is about 100μm wide and 34μm thick.

Electroepitaxy model

In the mathematical model of selective electroepitaxy presented in this study it is assumed that the solute transported to the advancing growth interface is removed from the solution only through

epitaxial growth on the substrate. The theoretical model developed by Bryskiewicz [12] for LPEE of multicomponent systems yields the following expression for the growth velocity

$$V = - \Delta T_0 f_1 + E f_2$$

where ΔT_0 is the change in interface temperature, primarily due to the Peltier cooling at the semiconductor-melt (S-M) interface, E is the electric field due to the electric current flow, f_1 and f_2 are functions of melt components and are independent of ΔT_0 and E. Under low current conditions and thin substrates, the interaction between the Peltier cooling on one side and the Peltier heating on the other side of the substrate is high (ΔT_0 can be neglected) and the growth is primarily due to the electric field E such as

$$V = E f_2$$

The above equation indicates that under controlled conditions, the layer uniformity is governed by the uniformity of the electric field along the S-M interface. To solve for the electric field, a mathematical model shown in figure 6 with the applied boundary conditions is used. The electric field is considered within the substrate bounded by the back contact melt on one side and the growth melt on the other side. The growth melt side is non-receptive for crystal growth except for a strip-like region of width w. A two dimensional Poisson's equation is considered for the mathematical analysis to solve for the electric field distribution in the substrate and along the substrate-melt interface.

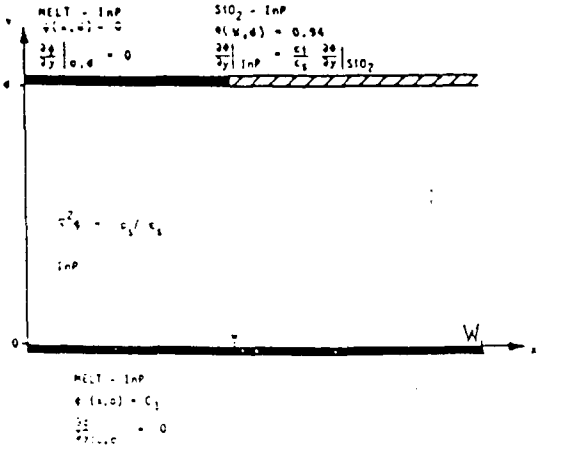

Figure 6. Schematic cross-section of the substrate, growth melt, and back contact melt, model used to analyze selective epitaxy.

The equation in two dimension is of the form

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = - \frac{\rho_s}{\varepsilon_s}$$

where ϕ, ρ_s, ε_s, are the electric potential total space-charge in the semiconductor and permittivity of the semiconductor respectively. The model is divided into three regions for the applied boundary conditions the back contact melt-InP region the growth melt-InP region, and the SiO_2-InP region. The electric field $\frac{\partial \phi}{\partial y}$ in the growth melt at $y \geq d$ and back contact melt $y \leq 0$ is

$$\frac{\partial \phi}{\partial y} = \frac{J}{\sigma}$$

where J is the electric current density and σ is the conductivity of the melt. If one assumes an ideal metal (the In melt), σ is very large and for small current density $\frac{\partial \phi}{\partial y}$ is approximately equal to zero. At the SiO_2-InP interface, the electric field is proportional to the ratio of permittivities such as

$$\left.\frac{\partial \phi}{\partial y}\right|_{InP\text{-}SiO_2} = \frac{\varepsilon_i}{\varepsilon_s} \left.\frac{\partial \phi}{\partial y}\right|_{SiO_2}$$

where ε_i is the insulator permittivity and ε_s is the InP permittivity. For $\phi(x,0) = 1.0$ volt and an oxide thickness of 2800 Å, $\left.\frac{\partial \phi}{\partial y}\right|_{SiO_2}$ is approximately equal to 3.57 V/μm and $\left.\frac{\partial \phi}{\partial y}\right|_{InP\text{-}SiO_2}$ is calculated to be about 1.12V/μm. The electric potential along the substrate-growth-melt interface is set to 0.0 volt, and at x = W, y = d, $\phi(W,d) = \phi(x,0) - I R_{sub}$. For I = 1.0A and R_{sub} = 60 mΩ $\phi(W,d)$ is about 0.94 V.

The total space-charge ρ_s in the substrate is given by

$$\rho_s = -q(n - p + N_D^*)$$

where q, n, p, and N_D^* are the elementary charge, electron density, hole density, and ionized impurities from deep levels, respectively. Since $n = p = n_i$ at the growth temperature (640°C), then

$$\rho_s = -qN_D^*$$

where N_D^* range from over $6 \times 10^{15}/cm^3$ to nearly $4 \times 10^{16}/cm^3$.

A finite element method is applied to the solution of Poisson's equation over the defined model. The equipotential and field cantour plots for narrow strip and wide strip geometries are shown in figures 7 and 8.

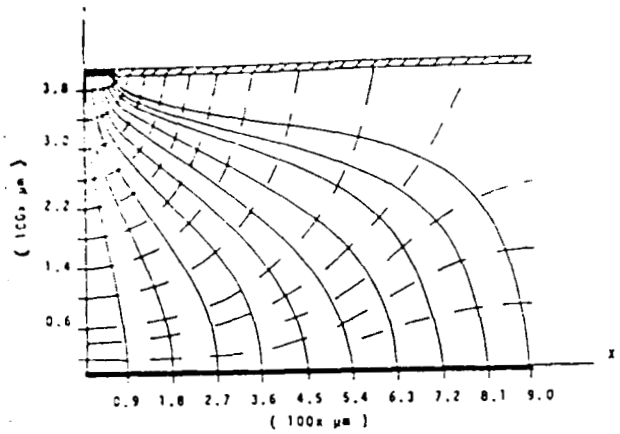

Figure 7. Equipotential and electric-field contour plots for narrow strip geometry (½ section).

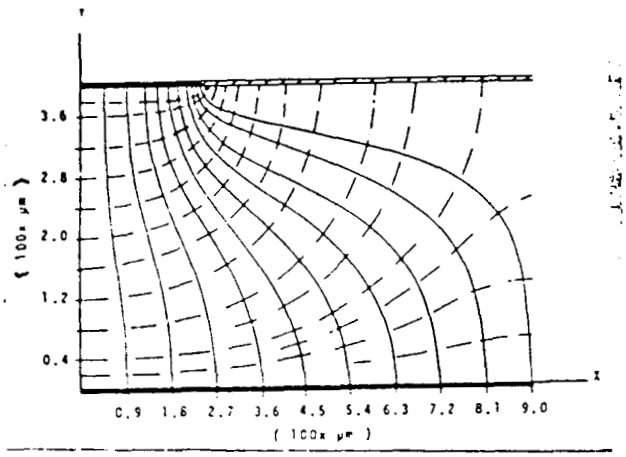

Figure 8. Equipotential and electric field contour plots for wide strip geometry (½ section).

Plots of the normalized field intensity along the growth melt-substrate interface for the two geometries is shown in figure 9. The field intensity is calculated using the equipotential contour plot closest to the strip and a grid increment of 20μm wide. The plots clearly show that the field intensity along narrow strip geometry is more uniform than in wide geometry.

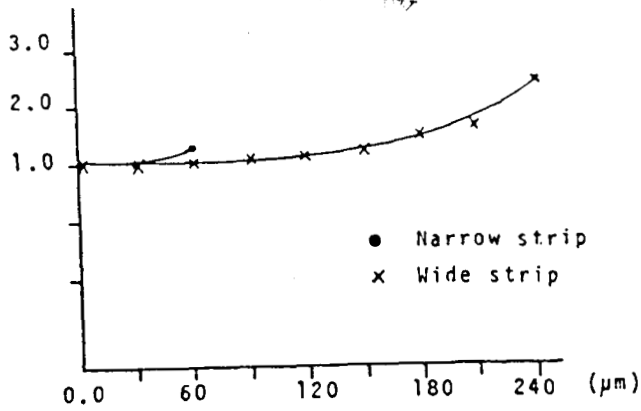

Figure 9. Normalized electric field intensity plots for narrow and wide geometries.

Conclusion

The computer simulation results show that the electric field intensity along the growth interface for narrow strip geometry is more uniform than in wide geometry. As a result, the layer grown on narrow strips were more uniform and have better surface morphology.

Acknowledgements

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